an insulated gate electrode in said trench, said insulated gate electrode comprising a gate insulating region on the trench sidewall and an electrically conductive gate on the gate insulating region, opposite the trench sidewall, said gate insulating region including a first insulating region of first thickness extending between said channel region and said electrically conductive gate and a second insulating region of second thickness extending between said drift region and said electrically conductive gate, and wherein the second thickness is greater than the first thickness; and

wherein said drift region has a linearly graded first conductivity type doping concentration therein which decreases from greater than about 1×10^{17} cm^{-3} to less than about 5×10^{16} cm^{-3} in a direction from said drain region to said channel region.

2. The field effect transistor of claim **1**, wherein a thickness of the gate insulating region adjacent the channel region is less than about 1000 Å and wherein a thickness of the gate insulating region adjacent the drift region is greater than about 1000 Å.

3. The field effect transistor of claim **1**, wherein a thickness of the gate insulating region adjacent the channel region is less than about 750 Å and wherein a thickness of the gate insulating region adjacent the drift region is greater than about three times the thickness of the gate insulating region adjacent the channel region.

4. The field effect transistor of claim **3**, wherein said channel region has a thickness less than 0.6 μm between the first P-N junction and the second P-N junction.

5. A field effect transistor, comprising:

semiconductor substrate having first and second opposing faces:

source region of first conductivity type in said substrate, adjacent the first face;

a drain region of first conductivity type in said substrate, adjacent the second face;

a drift region of first conductivity type in said substrate, said drift region extending between said drain region and said source region and having a graded first conductivity type doping concentration therein which decreases in a direction from said drain region to said source region;

a channel region of second conductivity type in said substrate, said channel region extending between said source region and said drift region and forming first and second P-N junctions therewith, respectively;

a trench in said substrate at the first face, said trench having a sidewall extending adjacent said drift region and said channel region; and

an insulated gate electrode in said trench, said insulated gate electrode comprising a gate insulating region on the trench sidewall and an electrically conductive gate on the gate insulating region, opposite the trench sidewall, said gate insulating region including a first insulating region of first thickness extending between said channel region and said electrically conductive gate and a second insulating region of second thickness extending between said drift region and said electrically conductive gate, and wherein the second thickness is greater than the first thickness; and

wherein said drift region has a first conductivity type doping concentration therein which decreases monotonically from a level greater than about 1×10^{17} cm^{-3} to less than about 5×10^{16} cm^{-3} in a direction from said drain region to said channel region.

6. A field effect transistor, comprising:

a semiconductor substrate having first and second opposing faces;

a source region of first conductivity type in said substrate, adjacent; the first face;

a drain region of first conductivity type in said substrate, adjacent the second face;

a drift region of first conductivity type in said substrate, said drift region extending between said drain region and said source region and having a graded first conductivity type doping concentration therein which decreases in a direction from said drain region to said source region;

a channel region of second conductivity type in said substrate, said channel region extending between said source region and said drift region and forming first and second P-N junctions therewith, respectively;

first and second trenches in said substrate at the first face, said trenches defining a mesa therebetween containing said source and channel regions and having respective facing sidewalls which extend adjacent said drift, channel and source regions; and

an insulated gate electrode in said first trench, said insulated gate electrode comprising a rate insulating region on the first trench sidewalls and an electrically conductive gate on the gate insulating region, opposite the first trench sidewall, said gate insulating region including a first insulating region of first thickness extending between said channel region and said electrically conductive gate and a second insulating region of second thickness extending between said drift region and said electrically/conductive gate, and wherein the second thickness is greater than the first thickness;

wherein the first conductivity type doping concentration of said drift region is less than about 2×10^{16} cm^{-3} at the second P-N junction;

wherein said drift region forms a non-rectifying junction with said drain region and wherein the first conductivity type doping concentration of said drift region is no less than about 1×10^{17} cm^{-3} at the non-rectifying junction; and

wherein a product of a distance between the facing sidewalls of said first and second trenches and the first conductivity type doping concentration of said drift region at the non-rectifying junction is between 1×10^{13} atoms cm^{-2} and 2×10^{13} atoms cm^{-2}.

7. The field effect transistor of claim **6**, wherein a product of a distance between the facing sidewalls of said first and second trenches and the first conductivity type doping concentration of said drift region at the second P-N junction is between 1×10^{11} dopant atoms cm^{-2} and 2×10^{12} dopant atoms cm^{-2}.

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